Gate-bias stress in amorphous oxide semiconductors thin-film transistors

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A quantitative study of the dynamics of threshold-voltage shifts with time in gallium-indium zinc oxide amorphous thin-film transistors is presented using standard analysis based on the stretched exponential relaxation. For devices using thermal silicon oxide as gate dielectric, the relaxation time is 3×10^5 s at room temperature with activation energy of 0.68 eV. These transistors approach the stability of the amorphous silicon transistors. The threshold voltage shift is faster after water vapor exposure suggesting that the origin of this instability is charge trapping at residual-water-related trap sites. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3187532]

Amorphous gallium-indium zinc oxide (GIZO) thin-film transistors (TFTs) have attracted attention for their possible applications to flat, flexible, and transparent displays,[1–4] especially when processed at low temperatures. However, like the other TFTs' technologies, they also suffer from a stability phenomena known as gate-bias stress.[5,6] This effect manifests itself as a continuous increase in threshold voltage (V_{th}) when the gate bias is kept constant over time. This limits the application of these TFTs in demanding applications, such as active matrix organic light emitting displays. The increase in V_{th} lowers the luminance of individual pixels over time, causing display nonuniformity.[7] As an example, using current technologies several driving transistors per pixel are necessary to compensate for the V_{th} shift. Hence, a proper understanding of the stressing mechanism is of paramount importance.

Gate-bias stress effects are commonly reported in the literature for a variety of transistors, *a*-Si TFTs,[8] organic transistors,[9–11] and recently also in amorphous oxide semiconductors TFTs.[12–15] The effect has been explained as a slow trapping of charge carriers in defects of unknown origin located at the semiconductor/dielectric interface.[13] It is known that the current degradation is faster when the devices are exposed to atmosphere[15,16] and that the stability improves after annealing.[1] Also, it has been reported that the effects can be reduced by the insertion of a passivation layer, either between the dielectric and the semiconductor[17] or on top of the semiconductor in bottom-gate structures.[16]

This work provides a quantitative study of the gate-bias stress instability as a function of temperature and environment conditions. The results allow a comparison with competing TFTs technologies. Furthermore, it also provides evidences that water vapor contamination enhances this instability. Therefore, there is no conceptual limitation for the stability of GIZO based TFTs. This is in contrast to hydrogenated amorphous silicon TFTs where the instability is caused by the creation of intrinsic defects, unsaturated valence states into which electrons are trapped.

The device fabrication process has been described in detail elsewhere.[18] Briefly, the TFTs were produced with a staggered bottom gate configuration on silicon wafers, which acted as the gate electrode. 100 nm thick SiO_2 produced either by (a) thermal oxidation or by (b) plasma enhanced chemical vapor deposition (PECVD) was used as the dielectric. A 40 nm thick GIZO (1:2:2 mol of Ga_2O_3:In_2O_3:ZnO) film was deposited at room temperature by rf magnetron sputtering, serving as the active channel layer. Finally, Ti/Au source/drain electrodes were e-beam evaporated with typical channel width and length of 50 and 25 μm, respectively. The GIZO active layer and the source/drain electrodes were patterned using the lift-off technique. The effect of annealing was studied by measuring both as-grown and annealed devices, being the annealing performed in a tubular furnace for 1 h, in air, at 200 °C. Wet-atmosphere exposure was carried out by bubbling dry N_2 through distilled water poured into a sealed flask. After this, the sample chamber was pumped to high vacuum for one hour prior to any electrical measurements.

Electrical measurements were carried out using a Keithley 487 picoammeter/voltage source. Measurements were carried out in dark conditions, in air as well as in high vacuum. Before stressing, the devices have a V_{th} in the range of 1–3 V. All the transistors work in accumulation mode.

Stress was measured as a function of time and temperature. As a typical example linear transfer curves are presented in the inset of Fig. 1 as a function of stress time. The device was fabricated using thermal SiO_2 as gate dielectric and it was annealed at 200 °C, being all the measurements done in vacuum. The applied gate bias during stress was 10 V and the transfer curves were measured in the linear region at a drain bias of 0.5 V. The gate-bias induced stress does not affect significantly the μ_{FE}, which is readily confirmed by the observation that the transistor transfer curves shift in a parallel fashion. However, it can be noticed that the curves were not perfectly linear over the entire voltage range.

Assuming that the threshold-voltage shift (ΔV_{th}) is due to trapped charges with surface density N_{tr}, ΔV_{th} is then given $\Delta V_{th}=eN_{tr}/C_{ox}$, where C_{ox} is the capacitance of the gate dielectric and e is the elementary charge. These trapped charges create an electric field that has to be compensated by the gate bias before an accumulation layer can be formed. The rate at which the charges are trapped depends on the free carrier concentration N_f. For an exponential distribution of trap states characterized by a temperature T_0, ΔV_{th} at infinite

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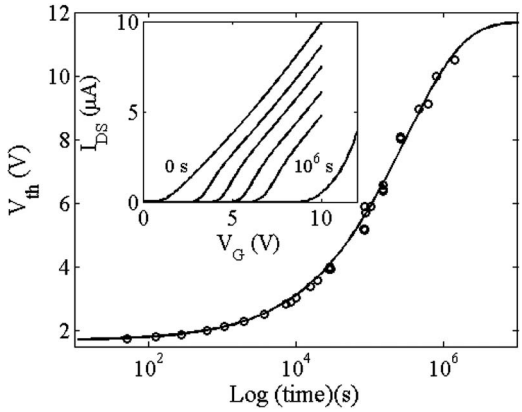

FIG. 1. V_{th} as function of time on a logarithmic scale. The continuous curve is a fit with stretched-exponential time dependence. The inset shows the drain current in the linear region (V_{DS}=0.5 V) as a function of the applied gate bias for increasing stress time. The gate bias during stress was 10 V and the temperature 20 °C.

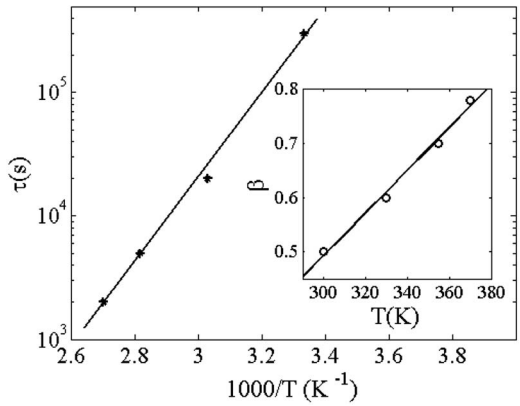

FIG. 2. τ as a function of reciprocal temperature. The line shows that τ is thermally activated with E_a=0.68 eV. The inset shows the corresponding β as a function of temperature.

stress time is equal to the applied gate bias, yielding a stretched exponential decay for V_{th} with time,

$$\Delta V_{th}(t) = V_0\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\},$$

where τ is a characteristic time constant, the dispersion parameter β equals T/T_0, and $V_0 = V_G - V_{th0}$, where V_{th0} is the threshold voltage at the start of the experiment. The relaxation time is thermally activated as

$$\tau = \upsilon^{-1}\exp\left(\frac{E_a}{k_B T}\right),$$

where E_a is the mean activation energy for trapping and υ is the frequency prefactor. This formalism allows the quantification of the device stability and is irrespective of the microscopic details of the process involved.[19]

The V_{th} is presented as a function of time on a logarithmic scale in Fig. 1. V_{th} saturates with time being the maximum shift equal to the applied gate bias. The continuous line is a fit to a stretched exponential. Perfect agreement is obtained for $\tau = 3\times10^5$ s and β=0.5 yielding a characteristic temperature of the trap states (T_0) of 600 K. A similar agreement was found for stress measurements at other temperatures (see Table I).

To further investigate the trapping dynamics, stress measurements were performed at various temperatures, in vacuum, using annealed TFTs with thermal SiO_2. The characteristic relaxation times are presented as a function of reciprocal temperature in Fig. 2. A straight line is obtained showing that the relaxation time is thermally activated, with E_a=0.68 eV and $\upsilon = 10^6$ s^{-1}. The inset of Fig. 2 shows the values of β as a function of temperature. E_a can be related to the microscopic nature of the trap site.

In spite of being recently observed that the gate-bias stress effect in TFTs can be reduced by protecting the transistors against environmental humidity, either with an encapsulation layer or by operating the transistor in vacuum,[15–17] a correlation between stability and contamination by water has never been established. In order to study this relation we measured and compare the stability of the annealed sample before and after water vapor exposure for 24 h. Figure 3 shows the relative threshold voltage shift $[V_{th}^{rel} = (V_{th} - V_{th0})/(V_g - V_{th0})]$. After water contamination, V_{th} increases with time much faster than before water vapor exposure. The continuous lines in Fig. 3 are fits to a stretched exponential. From these fits we obtain for τ a value that decreases one order of magnitude from $\tau = 3\times10^5$ to 3.9×10^4 s, while β remains approximately constant (~0.5). The fitting parameters are shown in Table I.

Water vapor exposure also causes a small change in the initial V_{th} (unstressed device), changing from 1.1 to 0.8 V. Therefore, the curves cross each other if V_{th} is represented in

TABLE I. Activation energy E_a, relaxation time τ, and dispersion parameter, β, at room temperature for investigated transistors, as well as for organic and silicon transistors. The table contains both our data as well as literature data. Values are presented for gate-bias stress in accumulation and recovery.

Semiconductor dielectric/processing		τ @RT (s)	β	E_a (eV)	Ref.
GIZO annealed @ 200 °C thermal SiO_2, stress in vacuum		3.0×10^5	0.5	0.68	This work
GIZO annealed @ 200 °C PECVD SiO_2 (measured in air)	Stress	1.2×10^5	0.5		This work
	Recover	4×10^2	0.12		
GIZO as-grown PECVD SiO_2 (measured in air)	Stress	1.4×10^3	0.5		This work
	Recover	4×10^4	0.4		
GIZO, thermal SiO_2 annealed @ 300 °C	Stress	2×10^4	0.42	0.53	13
GIZO, thermal SiO_2 annealed @ 300 °C	Stress	2×10^4			14
	Recover	3×10^5			
Organic semiconductor (in vacuum)		1×10^7	0.44	0.6	10
Organic semiconductor (in air)		1×10^4	0.5		11
Amorphous silicon	Stress	8×10^7		0.98	19
	Recover	5×10^9		1.1	
Microcrystalline silicon		10^{12}		1.07	6

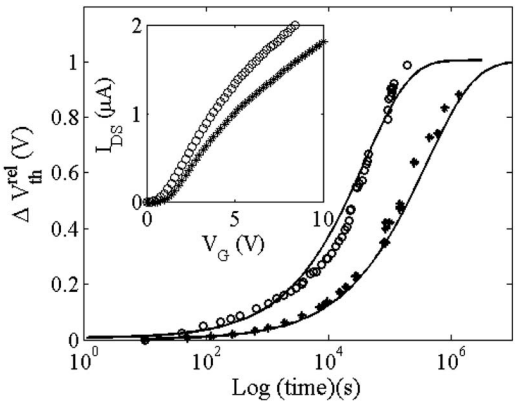

FIG. 3. V_{th}^{rel} measured before (*) and after (○) water vapor exposure. The continuous curves are a fit with stretched-exponential time dependence. Fitting parameters are in Table I. The inset shows the corresponding changes in the linear transfer curves measured for V_{DS}=0.5 V. The results were obtained in a device using thermal SiO_2 as gate dielectric and previously annealed at 200 °C.

absolute values. To avoid this crossing effect we chose to represent in Fig. 3 the relative threshold voltage shift (V_{th}^{rel}).

The linear transfer curves before and after the exposures to humidity are shown in the inset of Fig. 3. After water vapor contamination V_{th} decreases from 1.1 to 0.8 V and the μ_{FET} improves slightly from 5 to 6 cm^2/V s. These small changes, corresponding to a slight improvement on the device performance, can be the result of surface adsorbed water which still remains after pumping in vacuum. This water causes the formation of a surface accumulation layer of electrons.[15] However, water which diffuses toward the interface SiO_2/GIZO may act as a deep carrier trap leading to V_{th} degradation as observed in our experimental results. In contrast, it has been reported that the presence of water during annealing improves the transistor parameters.[20] In this case, the combined effect of water and oxygen at high temperatures passivates unstable bonds or carrier defects.[20]

Gate-bias stress experiments were also carried out on devices fabricated using SiO_2 grown by PECVD as a gate dielectric. Thermal annealed devices showed a significant higher stability than the as-grown devices (see Table I). In view of the previous results, the improvement of the device stability is possibly caused by the out-diffusion of water from the device.

To benchmark the stability of GIZO based transistors we have included in Table I the parameters τ, β, and E_a for other TFTs' technologies. The relaxation time of an annealed transistor is approaching the *a*-Si transistors. Also, since *a*-Si and μc-Si TFTs have activation energy higher than GIZO based TFTs, the difference in stability becomes less pronounced at high temperatures. Our data also shows a relaxation time of 3×10^5 s, which is one order of magnitude higher than the best value reported in the literature (2×10^4 s) for a GIZO based transistor produced using thermal SiO_2 as a gate dielectric[13,14] (see Table I).

In applications such as active matrix displays, the transistor is only temporarily switched on. The generated ΔV_{th} relaxes in the off-state. Recovery of stress is, therefore, as important as stress. The ΔV_{th} recover was studied by keeping the drain and the gate terminals grounded between the measurements of the transfer curves. Measurements were done on devices using PECVD SiO_2 as a gate dielectric. The ΔV_{th} is completely reversible and follows stretched-exponential time decay. Table I shows that for the as-grown device, the relaxation time for stress is slightly smaller than for recovery. However, recovering is much faster in the annealed device. This behavior is different from the previous reported for GIZO based transistor where V_{th} recovering is observed to be slower than stressing,[14] as well as on *a*-Si transistors where stress is orders of magnitude faster than recovery (see Table I).

In summary, we have investigated the stability of amorphous oxide TFTs using GIZO as the semiconductor channel layer. The Vth with time according to a stretched exponential. The relaxation times are thermally activated with activation energy of 0.68 eV for thermal SiO_2. Differences in stability are due to differences in the relaxation time that varies between 10^2 and 10^5 s. The gate-bias stress is completely reversible. Experiments after water vapor exposure clarifies previously reported results, demonstrating that water contamination increases significantly the gate-bias stress instability.

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