Resistive Random Access Memories (RRAMs) Based on Metal Nanoparticles

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Abstract. It is demonstrated that planar structures based on silver nanoparticles hosted in a polymer matrix show reliable and reproducible switching properties attractive for non-volatile memory applications. These systems can be programmed between a low conductance (off-state) and high conductance (on-state) with an on/off ratio of 3 orders of magnitude, large retention times and good cycle endurance. The planar structure design offers a series of advantages discussed in this contribution, which make it an ideal tool to elucidate the resistive switching phenomena.

Keywords: Nanoparticles, resistive switching, non-volatile memory.

1 Introduction

Non-volatile memories (NVMs) have become a major technology in the storing of digital information. Flash memory is currently the main stream of the non-volatile memory technology and can be found everywhere in our daily life particularly in portable devices. The absence of mechanical parts, lighter weight and lower power dissipation makes flash NVMs ideal for these applications. In flash memories the information is stored in the form of charge contained in a so-called floating gate (FG) completely surrounded by a dielectric (hence the name and located between the channel region and the conventional, externally accessible, gate of a field effect device (FET)). The amount of charge stored on the FG layer can be easily sensed since it is directly proportional to the threshold voltage of the FET. Flash retention relies on charge-storing on a floating gate, and this lays a challenge for the scaling-down. For instance, less than 100 electrons will be stored in 32 nm node, the information will be easily lost due to the leakage through the thin dielectric. Furthermore, as CMOS scaling proceeds, there is an increasing need to simplify and unify different technologies. In fact, to improve system performance, circuit designers often combine several memory types, adding complexity and cost. The unification of these different technologies would allow further scaling and the decrease of the system cost. Many of the memory caches in the hierarchy of today's computer architecture could be eliminated, reducing cost and complexity. Ideally, the ultimate universal memory aims to replace conventional embedded and stand-alone memories. Alternative routes to traditional memories are thus under intense investigation, with new NVM concepts and storage principles being investigated that may overcome the intrinsic limitation of flash and allow unification of existing memories. A variety of next generation NVMs has been proposed, from which Resistive Random Access

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Memory (RRAMs) are the latest. RRAMs are being intensively investigated by companies and universities worldwide. The main advantages offered by the technology are higher packing density, faster switching speed and longer storage life. The appeal of RRAM is that each element is a two-terminal device. Switching between high and low resistance is achieved by means of an appropriate electrical pulse, and the read-out process consists of applying a (lower) voltage to probe the state of the resistance. This type of element can be incorporated into cross-point arrays. Resistive type memories are usually metal-insulator-metal (MIM) structures which show non-volatile electrically induced resistance variations of up to nine orders of magnitude. Insulating materials can be as diversified as CuO, CoO, ZnO, NiO, TiO_2, MgO, Al_2O_3, SiO_2, perovskites, among others [1-6]. Thin films incorporating metallic nanoparticles (NPs) also show reliable and reproducible switching properties. Nanoparticles can be capped into polymeric materials and stable solutions are readily available [7-9]. Thin films hosting a well-defined distribution of nanoparticles are easily fabricated by spin-coating, printing, or dip-coating techniques offering the prospect of low fabrication cost, mechanical flexibility and lightweight.

2 Technological Innovation for Sustainability

Together with development of the microelectronic industry, the research on low power, low cost, and high density memory devices is necessary for the digital systems, especially for the portable systems. For instance, the absence of mechanical parts, lighter weight and lower power dissipation makes flash non-volatile memory ideal for these applications. However, flash retention relies on charge-storing on a floating gate, and this lays a challenge for the scaling-down. In this work we demonstrate a memory device, which makes use of thin polymer film hosting a matrix of silver nanoparticles. With on/off ratio as high as 10^3, a large retention time and good cycle endurance, the nanoparticles based device is a serious candidate to replace currently available non-volatile memories, and is able to improve all the relevant components as a reliable memory device.

Planar structures have a significant lower intrinsic capacitance than sandwich-type structures commonly reported; therefore, they should have a faster dynamic response. In addition, these co-planar structures have the active layer directly exposed and can be probed by a number of surface analytical techniques to identify and characterize topographical, morphological changes that occur in the devices upon resistive switching.

3 System Description

The colloidal solution of PolyVinylPyrolidone(PVP) capped- Silver nanoparticles was deposited on top of preformed gold microelectrode arrays fabricated on thermal oxidized silicon wafers. The interdigitated gold microelectrode arrays were separated apart 10 μm and 10.000 μm long. The samples were dried at room temperature for several hours for removal of the solvent. Prior to electrical measurements the samples were also pumped in vaccum to remove further any residual solvent. Electrical measurements were carried out using a Keithley 487 picoammeter/voltage source in dark conditions, high vacuum. Figure 1 shows the device test structure used to measure the electrical properties of the system comprised of nanocrystals in a semi

insulating or insulating host matrix. A thin film is formed between the two gold electrodes on top of the insulating silicon dioxide surface by drop casting or by spin coating. During all the measurement the conductive silicon substrate is kept grounded to prevent charging of the SiO_2 layer.

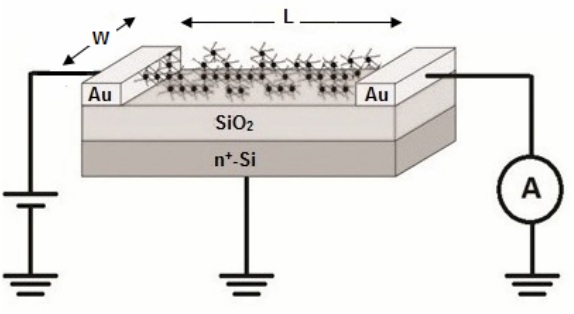

Fig. 1. Planar device structure with two gold electrodes. The device dimensions are W=10.000µm and L=10µm.

3.1 Current-Voltage Characteristics

Before the devices show resistive switching behavior, they have to undergo a forming process that is induced by applying a high bias voltage. In practice, forming voltages are typically ~50V. After forming the device exhibits the bistable current-voltage characteristics represented in Fig. 2. A low conductance state named off-state and a high conductance state designated as on-state. The on-state has a symmetric negative differentially resistance (NDR) region located between 25 and 30 V. The memory can be switched between off and on-state by applying voltage pulses with amplitudes corresponding to the top and bottom of the NDR region, in Fig. 2 about 20 V and 40 V, respectively.

The device can be read out non-destructively using voltages < 10V. The programming voltages are larger than those observed in conventional sandwich capacitor-like devices because the distance between electrodes is also significant higher.

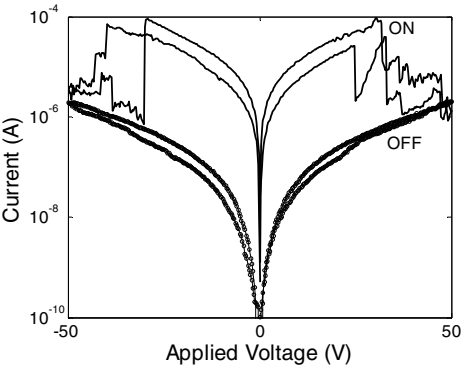

Fig. 2. Current-voltage characteristics showing the high conductance on-state and low conductance off-state

3.2 The Memory Characteristics

The nanoparticle based memory is nonvolatile, retaining the programmed conductance state for at least a week without any applied bias as long as they are stored in vacuum or in inert atmosphere. Fig.3 (a) shows the retention time for both states using a read voltage of 3 V.

Once the device is in a given memory state, it can be reliably read many times without degradation. Shown in Fig. 3(b) is a segment of the current response to write-read-erase-read voltage waveforms. The write voltage (W) is 35 V and the erase (E) is 50 V. For both states the read voltage (R) is 3V.

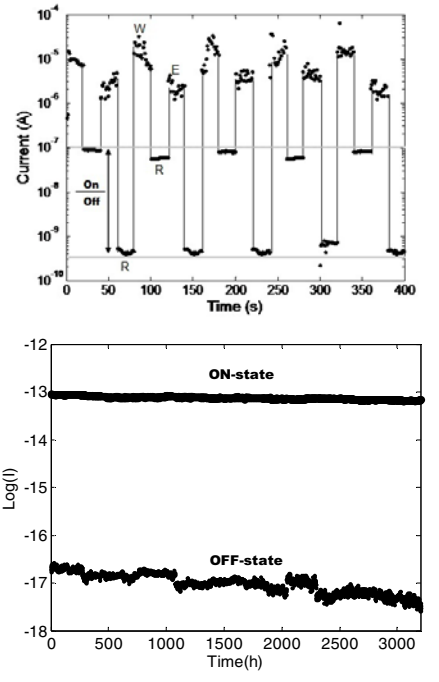

Fig. 3. (a) retention time of two memory states has been obtained at 3 volt. (b) typical current response to the write-read-rewrite-read voltage cycles. The write voltage (W) is 35 V and the erase (E) is 50 V. For both states the read voltage (R) is 3V.

4 Conclusion

Metal nanoparticles embedded in a polymer matrix exhibit the ability to switch between different nonvolatile conductance states. Programming of the memory states is done using voltage pulses. The memory device concept was demonstrated using a lateral structure with a large gap between electrodes (10μm). This structure needs substantially high programming voltages. However, it is feasible to bring the device dimensions to a nanometer scale and bring the magnitude of the operating voltages to values compatible with CMOS technology.

Since the basic active layer is a soluble polymer, large area arrays of memories can easily be fabricated into flexible substrates, thus opening the prospect for low-cost production of memory arrays for instance for radio-identification tags.

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