Errata for Master Thesis

Aging Sensor for CMOS Memory Cells

Hugo Fernandes da Silva Santos

Faro, 17th March of 2016

Page 44: Equation (7): $I_D = \frac{1}{2}\beta V_{DS}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)^2$, should be: $I_D = \frac{1}{2}\beta V_{DS}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)$

Page 64: Table 4.3 - Transition detector – Implementation 4, transistor sizes

Path	Inverter	Nmos	Pmos	L	V_{th_n}	V_{t_p}
1	Xinv1	5*WNmin	WPmin	65n	0.423V	-0.365V
	Xinv2	WNmin	5*WPmin			
	Xinv3	5*WNmin	WPmin			
	Xinv4	WNmin	5*WPmin			
2	Xinv1	5*WNmin	WPmin			
	Xinv2	WNmin	5*WPmin			
	Xinv3	5*WNmin	WPmin			
	Xinv4	WNmin	5*WPmin			

Should be:

Path	Inverter	Nmos	Pmos	L	V_{th_n}	V_{t_p}
1	Xinv1	5*WNmin	WPmin	65n	0.423V	-0.365V
	Xinv2	WNmin	5*WPmin			
	Xinv3	5*WNmin	WPmin			
	Xinv4	WNmin	5*WPmin			
2	Xinv1	WNmin	5*WPmin			
	Xinv2	5*WNmin	WPmin			
	Xinv3	5*WNmin	5*WPmin			
	Xinv4	5*WNmin	WPmin			

Page 69: "This connection allows to sum the transistor's parasitic capacitances cgs and cds to form a bigger capacitor." should be, "This connection allows to sum the transistor's capacitances cgs and cgd to form a bigger capacitor."